PATENT ABSTRACTS OF JAPAN

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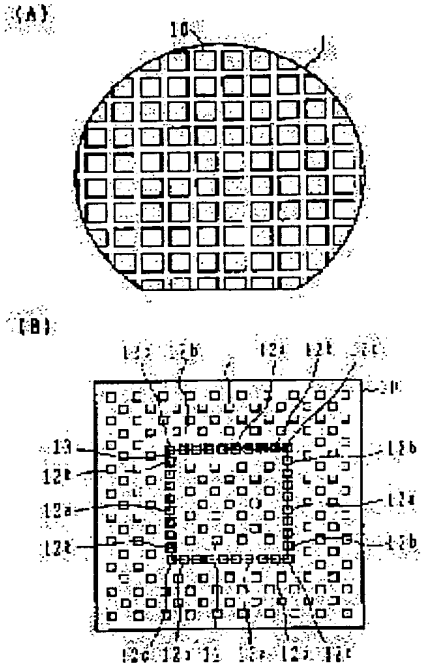
(54) SEMICONDUCTOR DEVICE AND ITS TESTING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To make it possible to reduce the voltage drop at the time of testing without lowering the integration degree by bringing a contact finger for supplying power into contact with a pad except the pad of the outermost periphery disposed in at least its chip area, and testing it.
SOLUTION: A semiconductor substrate 1 in which the surface formed with a plurality of chip areas 10 is provided, electronic circuits equivalent to each other are formed in the areas 10, and pads 11, 12a to 12c for taking electric connections with an electronic circuit in a chip area 10 and an external unit are disposed in two-dimensional manner on each area 10 is prepared. Contact fingers are brought into contact with the plurality of pads 12a to 12c of the part of one area 10 of the board 1, and the circuit formed in the area 10 is tested. In this case, the finger for supplying the power is brought into contact with the pad 12b except the pad of the outermost periphery disposed at least in the area 10, and tested.



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[Claim(s)]

[Claim 1] Have the front face where two or more chip fields were demarcated, and an electronic circuitry equivalent to mutual is formed in each chip field. The process for which the semi-conductor substrate with which the pad for taking the electrical installation of the electronic circuitry and external device which were formed in the chip field concerned for every chip field is arranged two-dimensional is prepared, It is the process which examines the electronic circuitry which the sensing pin was contacted to some two or more pads in one chip field of said semi-conductor substrate, respectively, and was formed in the chip field concerned. The test method of a semiconductor device including the process which examines by contacting the sensing pin for supplying a power source to pads other than the pad of the outermost periphery arranged in the chip field concerned at least.

[Claim 2] The test method of the semiconductor device according to claim 1 with which the process which performs said trial examines by contacting said sensing pin only to said pad for a trial including the pad for a trial which said pad arranged in each chip field of said semi-conductor substrate arranged along with the closed imagination line in each chip field, and the pad for actuation arranged to said closed contrant region and closed external field of a line.

[Claim 3] When are the semiconductor chip with which the electronic circuitry was formed in the interior, it exposes to the front face of said semiconductor chip, it arranges along with the closed imagination line in a front face and an internal electronic circuitry is examined The semiconductor device which has the pad for a trial which performs electrical installation of this electronic circuitry and an external device, and the pad for actuation which is exposed to the front face of said semiconductor chip, is arranged to said closed contrant region and closed external field of a line, and performs electrical installation of an internal electronic circuitry and an external device.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a semiconductor device and its test method.

[0002]

[Description of the Prior Art] The pad for performing electrical installation with the exterior came to be arranged two-dimensional on a chip front face with high integration of a semiconductor integrated circuit, and large-area-izing. The pad for a trial for examining the electronic circuitry of such a semiconductor chip is arranged at the edge of a semiconductor chip.

[0003] A sensing pin is contacted to the pad for a trial, a power source is supplied from the pad for current supply among the pads for a trial, a stimulus is sent and received through the pad for signal transmission and reception, and an electronic circuitry is examined.

[0004]

[Problem(s) to be Solved by the Invention] If a chip size is enlarged, the distance from the pad for a trial arranged by the outermost periphery to the core of a chip will become long. Moreover, when a pad is arranged two-dimensional, since a power source can be supplied also from the inner inner of a chip, it is lacking in the need of forming power-source wiring into low resistance, and positive low resistance-ization of power-source wiring may not be attained. For this reason, when supplying a power source from the pad for a trial of the outermost periphery, the voltage drop by resistance of power-source wiring becomes a big problem.

[0005] It is contrary to the request of high integration to expand the width of face of power-source wiring, in order to reduce a voltage drop. The object of this invention is offering the semiconductor device which can reduce the voltage drop at the time of a trial, and its test method, without reducing a degree of integration.

[0006]

[Means for Solving the Problem] According to one viewpoint of this invention, it has the front face where two or more chip fields were demarcated. The process for which the semi-conductor substrate with which the pad for taking the electrical installation of the electronic circuitry and external device which the electronic circuitry equivalent to mutual was formed in each chip field, and were formed in the chip field concerned for every chip field is arranged two-dimensional is prepared, It is the process which examines the electronic circuitry which the sensing pin was contacted to some two or more pads in one chip field of said semi-conductor substrate, respectively, and was formed in the chip field concerned. The test method of a semiconductor device including the process which examines by contacting the sensing pin for supplying a power source to pads other than the pad of the outermost periphery arranged in the chip field concerned at least is offered.

[0007] Since a power source is supplied from pads other than the pad of the outermost periphery at the time of the trial of a chip, the distance from the pad for current supply to each point in a chip field can be shortened. For this reason, the voltage drop by resistance of power-source wiring can be reduced.

[0008] When according to other viewpoints of this invention are the semiconductor chip with which the electronic circuitry was formed in the interior, it exposes to the front face of said semiconductor chip, it arranges along with the closed imagination line in a front face and an internal electronic circuitry is examined The semiconductor device which has the pad for a trial which performs electrical installation of this electronic circuitry and an external device, and the pad for actuation which is exposed to the front face of said semiconductor chip, is arranged to said closed contrant region and closed external field of a line, and performs electrical installation of an internal electronic circuitry and an external device is offered.

[0009] Since pads other than the pad of the outermost periphery are used as the pad for a trial, a power source can be supplied from pads other than the outermost periphery at the time of the trial of a chip. For this reason, the die length of power-source wiring can be shortened and the voltage drop by resistance of power-source wiring can be reduced.

[0010]

[Embodiment of the Invention] Drawing 1 (A) shows the outline top view of a semi-conductor wafer. Two or more chip fields 10 arranged in the shape of a grid on the front face of the semi-conductor wafer 1 are demarcated. The electronic circuitry is formed in the front face of the semi-conductor wafer 1 in each chip field 10.

[0011] Drawing 1 (B) shows the outline top view of one chip field 10 of the semi-conductor wafer 1 shown in drawing 1 (A). On the front face of the chip field 10, the pad 11 for actuation and the pads 12a, 12b, and 12c for a trial for taking the electrical installation of an electronic circuitry and an external device are formed. Fields other than a pad are covered by the insulating protective coat.

[0012] The pads 12a-12c for a trial are arranged along with the periphery 13 of the imagination square demarcated inside the chip field 10. The pad 11 for actuation is arranged to the field of the both sides of the interior of the square periphery 13, and the exterior.

[0013] Pad 12c for touch-down is arranged among the pads for a trial at the top-most vertices of the square periphery 13, and pad 12b for supply voltage supply adjoins pad 12c for touch-down, and is arranged. Pad 12a for stimuli is arranged at the staging area of each side of the square periphery 13.

[0014] At the time of the trial of a chip, the head of two or more sensing pins attached in the probe card is contacted to the pads 12a-12c for a trial, respectively, and the electronic circuitry and test equipment in a chip are connected electrically. Touch-down potential is given to the sensing pin in contact with pad 12c for touch-down from test equipment, and supply voltage is given to the sensing pin in contact with pad 12b for supply voltage supply. Transmission and reception of a stimulus are performed by Hazama of test equipment and the electronic circuitry in a chip through the sensing pin in contact with pad 12a for stimuli.

[0015] Thus, in this example, the pads 12a-12c for a trial are arranged to not a edge but the inner inner of a chip field. Here, a edge means the thing of the field where the pad of the outermost periphery is arranged among the pads arranged two-dimensional, and an inner inner means the field where pads other than the pad of the outermost periphery have been arranged. Since the pads 12a-12c for a trial are arranged to the inner inner, a power source can be supplied to the point of the arbitration in the chip field 10 with comparatively short wiring from the object for supply voltage supply, and the pads 12b and 12c for touch-down. For this reason, the voltage drop at the time of a chip trial can be reduced.

[0016] In addition, if the object for supply voltage supply and the pad for touch-down are arranged only at the core of a chip field, since the distance from a core to a edge will become long, arranging in the location shifted from the core is desirable.

[0017] For example, when the pads 12a-12c for a trial are arranged in the location of the middle point of a segment to which the core and periphery of a chip field are connected and the pad for a trial of top-most vertices is carried out to touch-down, the furthest part which should supply a power source becomes the top-most vertices of the chip field corresponding to it from pad 12c for one touch-down. This distance is set to about 5.6mm when die length of one side of the chip field 10 is 16mm.

[0018] Like before, the case where the pads 12a-12c for a trial are arranged inside only about 0.2mm rather than the edge of a chip field is considered. When using as the pad for touch-down the pad located in the middle point of each side, the furthest part which should supply a power source takes the lead in a chip field from one pad for touch-down. This distance is set to about 7.8mm when die length of one side of the chip field 10 is 16mm.

[0019] When the two above-mentioned examples are compared, by arranging the pad for a trial to the inner inner of a chip field shows that the distance to the furthest part which should supply a power source from a pad can be shortened about 30% compared with the case where it arranges at a edge. In order to heighten this compaction effectiveness, as shown in drawing 1 (B), it is desirable to arrange the pad for a trial in the location of the middle point of a segment to which the core and edge of a chip field are connected.

[0020] Although drawing 1 (B) showed the case where a chip field was a square, not only when a

chip field is a square, but in the case of a rectangle, a parallelogram, and the other configurations of arbitration, the above-mentioned example is applicable. When a chip field is a rectangle, the pad for a trial is also arranged along with a rectangle pattern. The compaction effectiveness of power-source wiring can be heightened by carrying out the pad which adjoins the pad and it which are located at the top-most vertices of this rectangle pattern to the object for touch-down, and supply voltage supply.

[0021] Moreover, by arranging the pad for a trial to the inner inner of a chip field, it does not depend on a chip size but the arrangement pattern of the pad for a trial can be standardized. For example, if one side is a bigger chip than the square which is 8mm, the pad for a trial can be arranged along with a with an one-side square [about 8mm square] periphery. By not depending on a chip size but standardizing the array pattern of the pad for a trial, the chip of different size using the same probe card can be examined.

[0022] In drawing 1 (B), each pads 11, 12a-12c are about [100micrometerx100micrometer] magnitude, and spacing between pad 12a-12c for a trial which adjoin mutually is 50 micrometers or less. Moreover, spacing of Hazama of each pads 12a-12c for a trial and the pad 11 for actuation nearest to the pad concerned is about 100 micrometers. Thus, spacing of the pads for a trial is narrower than spacing of the pad for a trial, and the pad for actuation nearest to it, and, generally let it be spacing below abbreviation one half.

[0023] Moreover, as shown in drawing 1 (B), when the pad 11 for actuation is arranged two-dimensional in the chip field 10, generally flip chip bonding of the chip is carried out to an external substrate. In order to carry out flip chip bonding, let the pad 11 for actuation be the bump pad in which the climax sections, such as lead, were formed on the front face of a wiring layer. Since it does not connect with an external substrate, the pads 12a-12c for a trial are standard pads which the wiring layer of the chip maximum upper layer exposed.

[0024] Although the above-mentioned example explained the case where the pad for a trial was arranged to the inner inner of a chip field, only the pad for the object for touch-down and supply voltage supply may be arranged to an inner inner among the pads for a trial.

[0025] Drawing 2 shows the outline top view of the chip which has arranged only the pad for the object for touch-down, and supply voltage supply to the inner inner. The pads 12a-12c for a trial are arranged by parallel each side at the edge of the chip field 10. Pad 12b for a trial for supply voltage supply and pad 12c for a trial for touch-down are arranged near [which connects the core of the chip field 10, and the middle point of each side] the middle point of a segment. It is arranged so that the pad 11 for actuation may be distributed over other fields two-dimensional. Furthermore, the pad of ends is set to pad 12b for supply voltage supply, and pad 12c for touch-down among the pads for a trial arranged to parallel each side, respectively.

[0026] As shown in drawing 2 , the supply voltage drop at the time of a trial can be reduced by arranging some pads 12a-12c for a trial at the edge of a chip field, and arranging only the pad for the object for touch-down, and supply voltage supply also to an inner inner among the pads for a trial.

[0027] Although this invention was explained in accordance with the example above, this invention is not restricted to these. For example, probably, it will be obvious to this contractor for various modification, amelioration, combination, etc. to be possible.

[0028]

[Effect of the Invention] As explained above, according to this invention, buildup of the die length of wiring which supplies a power source at the time of the trial of a chip can be controlled. Thereby, the supply voltage drop at the time of a trial can be reduced.

[Brief Description of the Drawings]

[Drawing 1] It is the top view showing the outline of the semi-conductor wafer by the example of this invention, and a chip field.

[Drawing 2] It is the top view showing the outline of the chip field by other examples of this invention.

[Description of Notations]

1 Semi-conductor Wafer

10 Chip Field

11 Pad for Actuation

12a The pad for a trial for stimuli

12b The pad for a trial for supply voltage supply

12c The pad for a trial for touch-down